

AMENDMENT OF SPECIFICATION

Please replace the first paragraph at original page 12, lines 1 to 13, with the following amended paragraph:

The [Processing] processing details of the trench etch are as follows :[[.]] The film stack is comprised of a bi-layer hard mask termed, Top HM1, and Bottom HM2, and a inter-metal dielectric layer, IMD, under the bilayer hard mask. Therefore, [[The]] the combination of HM1/ HM2/ IMD stack ~~[[, inter-metal dielectric]]~~ consists of, which can be any one of these schemes:

HM1 HM2 ~~[[IMD]]~~ IMD

USG/ SiC or SiN/ Fluorine doped Oxide or SiO<sub>2</sub>

USG/ SiC / Carbon-doped Oxide

USG/ SiC / Organic based low-k dielectric

USG/ SiC / porous low-k dielectric

(Note: ~~[[where]]~~ USG, is undoped silicate glass for the HM1 layer, hard mask top layer, and can also ~~[[can]]~~ be a conventional SiO<sub>2</sub> film of thickness in the range from 1000 to 2000 Angstroms .)

Please replace the second paragraph at original page 15, lines 15 to 21, with the following amended paragraph:

For completeness, the following is a detailed reactive ion etch, RIE, processing scheme for trench etch making use of the advantages of the bi-layer hard mask. This serves as just one example that was developed and reduced to practice, for RIE gas mixtures comprised of:

Step 1:  $\text{CF}_4$  ☐ and Ar based for etching ☐ opening in the BARC, the bottom antireflection coating

Step 2:  $\text{CF}_4$  ☐ and  $\text{CHF}_3$  ☐ with Ar ☐ for etching through the HM1, the top hard mask layer ☐

Step 3:  $\text{N}_2$  ☐ and  $\text{O}_2$  ☐ for etching the via-fill material recess

Step 4:  $\text{CF}_4$  ☐ and  $\text{N}_2$  ☐ with  $\text{O}_2$  ☐ for etching the HM2, the bottom hard mask layer, and the IMD, inter-metal dielectric ☐

Step 5:  $\text{O}_2$  ☐ for Ashing

Step 6:  $\text{CHF}_3$  ☐ with  $\text{N}_2$  ☐ for bottom etch stop layer etch ☐